ABSTRACT

The information processing device in the present invention includes a memory 1 which is a DRAM featuring a burst mode, and burst-transfers data at successive column addresses, masters (13), (14), and (15) which issue access requests, and a command processing unit (11) which converts an access address that is included in the access request issued from each master. One or more of the masters access an M x N rectangular area where M and N are integers, and the command processing unit (11) converts access addresses so that a column address of data at the (K+m)th column, where K and m are integers and $m \leqq M$, of an Lth line, and a column address of data at a Kth column of an (L+n)th line, where L and n are integers and $n \leqq N$, become successive.